

PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH  
ASYMMETRICAL TUNNEL BARRIERS

Abstract of the Disclosure

5 Structures and methods for programmable array type logic and/or memory  
devices with asymmetrical low tunnel barrier intergate insulators are provided. The  
programmable array type logic and/or memory devices include non-volatile memory  
which has a first source/drain region and a second source/drain region separated by a  
channel region in a substrate. A floating gate opposing the channel region and is  
10 separated therefrom by a gate oxide. A control gate opposes the floating gate. The  
control gate is separated from the floating gate by an asymmetrical low tunnel  
barrier intergate insulator. The asymmetrical low tunnel barrier intergate insulator  
includes a metal oxide insulator selected from the group consisting of  $\text{Al}_2\text{O}_3$ ,  $\text{Ta}_2\text{O}_5$ ,  
 $\text{TiO}_2$ ,  $\text{ZrO}_2$ ,  $\text{Nb}_2\text{O}_5$ ,  $\text{SrBi}_2\text{Ta}_2\text{O}_3$ ,  $\text{SrTiO}_3$ ,  $\text{PbTiO}_3$ , and  $\text{PbZrO}_3$ . The floating gate  
15 includes a polysilicon floating gate having a metal layer formed thereon in contact  
with the low tunnel barrier intergate insulator. And, the control gate includes a  
polysilicon control gate having a metal layer, having a different work function from  
the metal layer formed on the floating gate, formed thereon in contact with the low  
tunnel barrier intergate insulator.

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